Claim 15 (previously presented) The semiconductor device of claim 14, wherein the first portion and the third portion of the first non-planar metallization level are connected.

Claim 16 (previously presented) The semiconductor device of claim 14, wherein between the first non-planar metallization level and the second planar metallization level an insulating layer is arranged, wherein in the insulating layer at least one through connection for a connection of the first non-planar metallization level to the second planar metallization level is formed.

Claim 17. (previously presented) The semiconductor device of claim 15, wherein the third portion implemented to shield the gate against electrostatic or electrodynamic interferences.

Claim 18 (previously presented) The semiconductor device of claim 15, wherein the predetermined displacement is set to be between about 250 nm and about 500 nm.

Claim 19. (previously presented) The semiconductor device of claim 18, and further comprising an oxide layer disposed between the third portion and the gate.

Claim 20. (previously presented) The semiconductor device of claim 19, and further comprising a reduced surface field area formed in the substrate and disposed between the gate and the drain area.

Claim 21. (previously presented) The semiconductor device of claim 14, wherein the predetermined displacement is set to be less than the thickness of the gate.